



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
(Case No. 00-167-C)

PATENT

In re Application of: )  
 )  
Werner, et al. )  
 ) Group Art Unit: 2819  
Serial No.: 09/742,250 )  
 )  
Filed: December 20, 2000 ) Examiner: L. Nguyen  
 )  
For: Apparatus and Method for )  
Improving Resolution of a )  
Current Mode Driver )

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RECEIVED  
NOV - 4 2003  
TECHNOLOGY CENTER 2800

Dear Sir:

Pursuant to 37 C.F.R. Section 1.97-1.98, and in accordance with the duty of candor set forth in 37 C.F.R. §1.56, applicants wish to make the following references of record in the above-identified application. Copies of the references cited below are enclosed along with a copy of completed PTO Form-1449 and fee pursuant to 37 C.F.R. § 1.97 (c) and 1.17(p).

**I. U.S. PATENTS**

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
1.	2,912,684	Steele	November 10, 1959
2.	3,051,901	Yaeger	June 24, 1958
3.	3,078,378	Burley et al.	June 28, 1960
4.	3,267,459	Chomicki et al.	December 18, 1962

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
5.	3,484,559	Rigby	July 28, 1966
6.	3,508,076	Winder	August 26, 1967
7.	3,510,585	Stone	February 2, 1967
8.	3,560,856	Kaneko	December 26, 1967
9.	3,569,955	Maniere	March 9, 1971
10.	3,571,725	Kaneko	March 23, 1971
11.	3,587,088	Franszek	June 22, 1971
12.	3,648,064	Mukai et al.	March 7, 1972
13.	3,697,874	Kaneko	October 10, 1972
14.	3,731,199	Tazaki et al.	May 1, 1973
15.	3,733,550	Tazaki et al.	May 15, 1973
16.	3,753,113	Maruta et al.	August 14, 1973
17.	3,754,237	de Laage de Meux	August 21, 1973
18.	3,761,818	Tazaki et al.	September 25, 1973
19.	3,772,680	Kawai et al.	November 13, 1973
20.	3,798,544	Norman	March 19, 1974
21.	3,832,490	Leonard	August 27, 1974
22.	3,860,871	Hinoshita et al.	January 14, 1975
23.	3,876,944	Mack et al.	April 8, 1975
24.	3,927,401	McIntosh	December 16, 1975
25.	3,978,284	Yoshino et al.	August 31, 1976
26.	3,988,676	Whang	October 26, 1976

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
27.	4,038,564	Hakata	July 26, 1977
28.	4,070,650	Ohashi et al.	January 24, 1978
29.	4,086,587	Lender	April 25, 1978
30.	4,097,859	Looschen	June 27, 1978
31.	4,131,761	Giusto	December 26, 1978
32.	4,181,865	Kohyama	January 1, 1980
33.	4,280,221	Chun et al.	July 21, 1981
34.	4,373,152	Jacobsthal	February 8, 1983
35.	4,382,249	Jacobsthal	May 3, 1983
36.	4,403,330	Meyer	September 6, 1983
37.	4,408,135	Yuyama et al.	October 4, 1983
38.	4,408,189	Betts et al.	October 4, 1983
39.	4,438,491	Constant	March 20, 1984
40.	4,481,625	Roberts et al.	November 6, 1984
41.	4,528,550	Graves et al.	July 9, 1985
42.	4,571,735	Furse	February 18, 1986
43.	4,602,374	Nakamura et al.	July 22, 1986
44.	4,620,188	Sengehanh	October 28, 1986
45.	4,628,297	Mita et al.	December 9, 1986
46.	4,748,637	Bishop et al.	May 31, 1988
47.	4,779,073	Iketani	October 18, 1988
48.	4,805,190	Jaffre et al.	February 14, 1989

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
49.	4,821,286	Graczyk et al.	April 11, 1989
50.	4,823,028	Lloyd	April 18, 1989
51.	4,825,450	Herzog	April 25, 1989
52.	4,841,301	Ichihara	June 20, 1989
53.	4,860,309	Costello	August 22, 1989
54.	4,875,049	Yoshida	October 17, 1989
55.	4,888,764	Haug	December 19, 1989
56.	5,003,555	Bergmans	March 26, 1991
57.	5,023,488	Gunning	June 11, 1991
58.	5,023,841	Akrout et al.	June 11, 1991
59.	5,045,728	Crafts	September 3, 1991
60.	5,046,050	Kertis	September 3, 1991
61.	5,115,450	Arcuri	May 19, 1992
62.	5,121,411	Flurharty	June 9, 1992
63.	5,126,974	Sasaki et al.	June 30, 1992
64.	5,153,459	Park et al.	October 6, 1992
65.	5,172,338	Mehrotra et al.	December 15, 1992
66.	5,191,330	Fisher et al.	March 2, 1993
67.	5,194,765	Dunlop et al.	March 16, 1993
68.	5,230,008	Duch et al.	July 20, 1993
69.	5,243,625	Verbakel et al.	September 7, 1993
70.	5,254,883	Horowitz et al.	October 19, 1993

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
71.	5,259,002	Carlstedt	November 2, 1993
72.	5,280,500	Mazzola et al.	January 18, 1994
73.	5,287,108	Mayes et al.	February 15, 1994
74.	5,295,155	Gersbach et al.	March 15, 1994
75.	5,295,157	Suzuki et al.	March 15, 1994
76.	5,315,175	Langner	May 24, 1994
77.	5,331,320	Cideciyan et al.	July 19, 1994
78.	5,373,473	Okumura	December 13, 1994
79.	5,408,498	Yoshida	April 18, 1995
80.	5,412,689	Chan et al.	May 2, 1995
81.	5,425,056	Maroun et al.	June 13, 1995
82.	5,426,739	Lin et al.	June 20, 1995
83.	5,459,749	Park	October 17, 1995
84.	5,471,156	Kim et al.	November 28, 1995
85.	5,473,635	Chevroulet	December 5, 1995
86.	5,483, 110	Koide et al.	January 9, 1996
87.	5,438,593	Karam et al.	August 1, 1995
88.	5,508,570	Laber et al.	April 16, 1996
89.	5,513,327	Farmwald et al.	April 30, 1996
90.	5,525,983	Patel et al.	June 11, 1996
91.	5,534,795	Wert et al.	July 9, 1996
92.	5,534,798	Phillips et al.	July 9, 1996

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
93.	5,539,774	Nobakht et al.	July 23, 1996
94.	5,553,097	Dagher	September 3, 1996
95.	5,596,439	Dankberg et al.	January 21, 1997
96.	5,608,755	Rakib	March 4, 1997
97.	5,633,631	Teckman	May 27, 1997
98.	5,663,663	Cao et al.	September 2, 1997
99.	5,640,605	Johnson et al.	June 17, 1997
100.	5,644,253	Takatsu	July 1, 1997
101.	5,684,833	Watanabe	November 4, 1997
102.	5,964,424	Ariyavisitakul	December 2, 1997
103.	5,734,294	Bezzam et al.	March 31, 1998
104.	5,740,201	Hui	April 14, 1998
105.	5,742,591	Himayat et al.	April 21, 1998
106.	5,751,168	Speed, III et al.	May 12, 1998
107.	5,757,712	Nagel et al.	May 26, 1998
108.	5,761,246	Cao et al.	June 2, 1998
109.	5,793,815	Goodnow et al.	August 11, 1998
110.	5,793,816	Hui	August 11, 1998
111.	5,796,781	DeAndrea et al.	August 18, 1998
112.	5,798,918	Georgiou et al.	August 25, 1998
113.	5,809,033	Turner et al.	September 15, 1998
114.	5,825,825	Altmann et al.	October 20, 1998

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
115.	5,864,584	Cao et al.	January 26, 1999
116.	5,867,010	Hinedi et al.	February 2, 1999
117.	5,872,468	Dyke	February 16, 1999
118.	5,887,032	Cioffi	March 23, 1999
119.	5,892,466	Walker	April 6, 1999
120.	5,898,734	Nakamura et al.	April 27, 1999
121.	5,917,340	Manohar et al.	June 29, 1999
122.	5,917,856	Torsti	June 29, 1999
123.	5,933,458	Leurent et al.	August 3, 1999
124.	5,942,994	Lewiner et al.	August 24, 1999
125.	5,946,355	Baker	August 31, 1999
126.	5,949,280	Sasaki	September 7, 1999
127.	5,969,579	Hartke et al.	October 19, 1999
128.	5,969,648	Garnett	October 19, 1999
129.	5,970,088	Chen	October 19, 1999
130.	5,973,508	Nowak et al.	October 26, 1999
131.	5,977,798	Zerbe	November 2, 1999
132.	5,982,741	Ethier	November 9, 1999
133.	5,986,472	Hinedi et al.	November 16, 1999
134.	6,005,895	Perino et al.	December 21, 1999
135.	6,006,169	Sandhu et al.	December 21, 1999
136.	6,009,120	Nobakht	December 28, 1999

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
137.	6,018,550	Emma et al.	January 25, 2000
138.	6,034,993	Norrell et al.	March 7, 2000
139.	6,038,260	Emma et al.	March 14, 2000
140.	6,048,931	Fujita et al.	April 11, 2000
141.	6,049,229	Manohar et al.	April 11, 2000
142.	6,052,390	Deliot et al.	April 18, 2000
143.	6,061,395	Tonami	May 9, 2000
144.	6,067,326	Jonsson et al.	May 23, 2000
145.	6,078,627	Crayford	June 20, 2000
146.	6,094,461	Heron	July 25, 2000
147.	6,097,215	Bialas, Jr. et al.	August 1, 2000
148.	6,101,561	Beers et al.	August 8, 2000
149.	6,114,979	Kim	September 5, 2000
150.	6,122,010	Emelko	September 19, 2000
151.	6,140,841	Suh	October 31, 2000
152.	6,160,421	Barna	December 12, 2000
153.	6,195,397	Kwon	February 27, 2001
154.	6,204,785	Fattaruso	March 20, 2001
155.	6,215,635	Nguyen	April 10, 2001
156.	6,222,380	Gerowitz	April 24, 2001
157.	6,307,824	Kuroda et al.	October 23, 2001
158.	RE 30,182	Howson	December 25, 1979



	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Issue Date</u>
159.	5,825,450	Date et al.	October 20, 1998
160.	5,604,468	Gillig	February 18, 1997
161.	5,546,042	Tedrow et al.	August 13, 1996
162.	6,094,075	Garrett, Jr. et al.	July 25, 2000
163.	6,069,577	Morisson et al.	May 30, 2000

## II. FOREIGN PATENTS

	<u>Patent Number</u>	<u>Inventor(s)</u>	<u>Publication Date</u>
164.	WO 95/31867	Lechleider	November 23, 1995
165.	WO 96/31038	Sikiguchi	October 3, 1996
166.	WO 99/10982	Garrett et al	March 4, 1999
167.	EP 0 352 869	Cowles et al.	January 31, 1990
168.	EP 0 482 392 (with translation)	Banniza	April 29, 1992
169.	EP 0 490 504	Fisher et al.	July 17, 1992
170.	EP 0 094 624	Meyer	November 23, 1983
171.	DE 43 20 930	Ludzuweit et al.	January 5, 1995
172.	JP 358070662	Kawasaki	April 27, 1983
173.	JP 362051329	Minami	March 6, 1987
174.	JP 354051343	Miyata	April 23, 1979
175.	JP 356164650	Nishitani et al.	December 17, 1981
176.	JP 359036465	Hideshima et al.	February 28, 1984
177.	JP 360087551	Torii	May 17, 1985

178.	JP 360194647	Nishino, et al.	October 3, 1985
179.	JP 408286943	Imai	November 1, 1996
180.	JP 409181778	Sakakura	July 11, 1997
181.	JP 354060850	Inoue	May 16, 1979
182.	JP 408202677	Hasegawa	August 9, 1996
183.	JP 405143211	Irie	June 11, 1993
184.	JP 404044691	Saito	February 14, 1992
185.	JP 402140676	Okayasu	May 30, 1990
186.	JP 402128201	Yatsuda	May 16, 1990
187.	JP 10200345	Yajima	July 13, 1998
188.	WO 98/33306	Fukuda	July 30, 1998
189.	EP 0 463 316	Biber	January 2, 1992
190.	JP 58-54412	Seisakusho	March 3, 1983

### III. OTHER DOCUMENTS

191. IEEE Standard 802.3ad-1999, 802.3 Supplemental. Local and Metropolitan Area Networks, July 17, 1999.
192. 802.3 ab., A Tutorial Presentation, 63 pages, presented at an IEEE 802.3 working group meeting in March 1998.
193. Thompson, "How 1000BASE-T Works", *IEEE802.3 Plenary*, (1997), Montreal PQ Canada, 8 pages
194. Perez-Alvarez, et al. "A Differential Error Reference Adaptive Echo Canceller for Multilevel PAM Line Codes", *IEEE*, pp. 1707-1710 (1996).
195. Kuczyski, et al., "A 1Mb/s Digital Subscriber Line Transceiver Signal Processor", *1993 IEEE International Solid-State Circuits Conference*, (1993)
196. Cova, et al. "Characterization of Individual Weights in Transversal Filters and Application to CCD's", *IEEE Journal of Solid-State Circuits*, Vol. SC-17, pp. 1054-1061 (1982).

197. Dally, et al., "Multi-Gigabit Signaling with CMOS", May 12, 1997.
198. Fielder, et al. "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," *1997 IEEE International Solid State Circuit Conference* and Slideset.
199. Raghavan, et al. "Nonuniformly Spaced Trapped Delay-Line Equalizers", *IEEE Transactions on Communications*, Vol. 41, pp. 1290-1295 (1993).
200. Ariyavisitakul, et al., "Reduced-Complexity Equalization Techniques for Broadband Wireless Channels", *IEEE Journal on Selected Areas in Communication*, pp. 5-15 (1997).
201. Ariyavisitakul, et al., "Tap-Selected Decision-Feedback Equalization", *IEEE Transactions on Communications*, pp. 1497-1500 (1997).
202. Sidiropoulos, et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 681-690 (1997).
203. Donnelly et al, "A 660 MB/s Interface Megacell Portable Circuit in 0.3  $\mu$ m-0.7  $\mu$ m CMOS ASIC", *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 1995-2003 (1996).
204. Allen, "Probability, Statistics, and Queueing Theory with Computer Science Applications," 2<sup>nd</sup> Edition, CH 7, pp.450-459.
205. Chappell, et al., "A 2ns-Cycle, 4ns Access 512kb CMOS ECL SRAM", *1991 IEEE Journal of Solid-State Circuits*, pp. 50-51 (1991).
206. Pilo, et al., "A 300MHz, 3.3V 1Mb SRAM Fabricated in a .5  $\mu$ m CMOS Process," *IEEE Journal of Solid-State Circuits*, pp. 148-149 (1996).
207. Schumacher, et al., "CMOS Subnanosecond True-ECL Output Buffer", *IEEE Journal of Solid-State Circuits*, Vol. 25, pp. 150-154 (1990).
208. Yang, et al., "A 4-ns 4Kx1-bit Two Port BiCMOS SRAM", *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1030-1040 (1988).
209. Bazes, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", *IEEE Journal of Solid State Circuits*, Vol. 28, pp. 165-168, (1991).
210. Ishibe, et al. "High-Speed CMOS I/O Buffer Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 27, pp. 671-677 (1992).
211. Lee, et al., "A 80ns 5V-Only Dynamic RAM", *ISSCC/79 Proceedings*, Paper 12.2 (1979).
212. Seki, et al., "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier", *IEEE Journal of*

*Solid-State Circuits*, Vol. 28, pp. 478-483 (1993).

213. Kobayashi, et al., "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture", *IEEE Journal of Solid State Circuits*, pp. 523-527 (1993).
214. Tomassini et al., "A fully differential CMOS Line Driver for ISDN", *IEEE Journal of Solid State Circuits*, Vol. 25, No. 2 (1990).
215. Farjad-Rad, et al., "A 0.4 $\mu$ m CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter", *IEEE Journal of Solid-State Circuits*, Vol. 34, pp. 580-585 (1999).
216. Yeung, et al., "A 2.4Gbps Per Pin Simultaneous Bidirectional Parallel Link with Per Pin Skew Compensation", *ISSCC 2000*, pp. 1-11.
217. Portmann et al., "A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRaMs", *IEEE VLSI Circuits Symposium*, June 1999.
218. Moncayo, "Bus Design and Analysis at 500 MHz and Beyond", *High Performance System Design Conference*, (1995).
219. Lau, et al. "A 2.6-Byte/s Multipurpose Chip-to-Chip Interface", *IEEE Journal of Solid State Circuits*, Vol. 33, pp. 1617-1626 (1998).
220. Current, "Current Mode CMOS Multiple-Valued Logic Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 2, pp. 95-107 (1994).
221. Dally and Poulton, *Digital Systems Engineering*, Cambridge University Press, New York, pp. 334-347 and 352 (1998).
222. Farjad-Rad, et al. "An Equalization Scheme for 10Gb/s 4-PAM Signaling over Long Cables," *Department of Electrical Engineering, Stanford University*, 1997.
223. IBM Technical Disclosure Bulletin, June 1967, "Use of Multibit encoding to increase Linear Recording Densities in Serially Recorded Records," pp. 14-15.
224. IBM Technical Disclosure Bulletin, Jan. 1968, "Coding Data Transmission," pp. 1295-1296.
225. IBM Technical Disclosure Bulletin, July 1969, "Clock Recovery Circuit," pp. 219-220.
226. IBM Technical Disclosure Bulletin, November 1970, "Transmission by Data Encoding", pp. 1519-1520.
227. IBM Technical Disclosure Bulletin, Feb. 1976, "Bidirectional Communications Within a

- Binary Switching System,” pp. 2865-2866.
228. IBM Technical Disclosure Bulletin, Feb. 1976, “Multilevel Bidirectional Signal Transmission,” pp. 2867-2868.
  229. IBM Technical Disclosure Bulletin, October 1978, “Multilevel Signal Transfers,” pp. 1798-1800.
  230. IBM Technical Disclosure Bulletin, Feb. 1981, “Circuit for Multilevel Logic Implementation,” pp. 4206-4209.
  231. IBM Technical Disclosure Bulletin, April 1983, “Multi Level Logic Testing”, pp. 5903-5904.
  232. IBM Technical Disclosure Bulletin, September 1985, “Push-Pull Multi-Level Driver Circuit for Input-Output Bus,” pp. 1649-1651.
  233. IBM Technical Disclosure Bulletin, Aug. 1986, “Multilevel CMOS Sense Amplifier,” pp. 1280-1281.
  234. IBM Technical Disclosure Bulletin, Nov. 1992, “Multi-Level Encoded High Bandwidth Bus,” pp. 444-447.
  235. IBM Technical Disclosure Bulletin, Feb. 1995, “High Speed Complimentary Metal Oxide Semiconductors Input/Output Circuits,” pp. 111-114.
  236. IBM Technical Disclosure Bulletin, April 1995, “Common Front End Bus for High-Performance Chip-to-Chip Communication,” pp. 443-444.
  237. IBM Technical Disclosure Bulletin, April 1995, “High Performance Impedance Controlled CMOS Driver,” pp. 445-448.
  238. IBM Technical Disclosure Bulletin, April 1995, “3-state Decoder for External 3-State Buffer,” pp. 477-478.
  239. Matlick, Transmission Lines for Digital and Communication Networks: An Introduction to Transmission Lines, High-Frequency and High-Speed Pulse Characteristics and Applications, IEEE Press, New York, pp. 268-269 (1995).
  240. Singh, “Four Valued Buses for Clocked CMOS VLSI Systems”, *Proceedings of the Seventeenth International Symposium on Multiple-Valued Logic, The Computer Society of the IEEE*, pp. 128-133 (1987).
  241. Smith, “The Prospects for Multivalued Logic: a Technology and Applications View”, *IEEE Transactions on Computers*, Vol. c-30, pp. 619-634 (1981).

242. Thrion, "10 Gig PMD Technologies," *IEEE Plenary*, Kauai, Hawaii, (1999).
243. Vranesic, "Multivalued Signalling in Daisy Chain Bus Control", *Proceedings of the Ninth International Symposium on Multiple-Valued Logic*, Bath, England, pp. 14-18 (1979).
244. Azadet et al., "A Gigabit Transceiver Chip Set for UTP CAT6 Cables in Digital CMOS Technology," *2000 IEEE International Solid State Circuits Conference*, pp. 3-6-307.
245. Yang, et al., "A Scalable 32Gb/s Parallel Data Transceiver with On-Chip Timing Calibration Circuits", *2000 IEEE International Solid-State Circuits Conference*, pp. 258-259 (2000).
246. Modulation Schemes for High Bit Rate Data Transmission in the Loop Plant, URL-<http://www.bib.fri-lippe.de/volltext/dipl/schlegd/chapter4.html>, 29 pages, printed 4/19/01.
247. Scott, "Propagation Over Multiple Parallel Transmission Lines Via Modes", IBM Technical Disclosure Bulletin, April 1990.
248. 1996 Symposium on VLSI Circuits, *IEEE*, June 13-15, 1996
249. Taborek, et al. IEEE 802.3 Tutorial, "Multi-Level Analog Signaling Techniques for 10 Gigabit Ethernet"
250. IBM, Servo Control of Analog Power Supplies Interface Card, 4/1/1993, Vol 36, Issue 4, pp. 283-286.

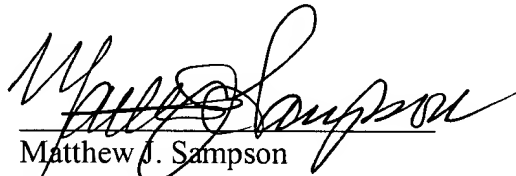
#### **IV. Discussion**

In regard to the foregoing references, many pertain to the general state of the art. Others have been cited in regard to related applications. In particular, reference numbers 1-39, 41-44, 47-74, 76-90, 94, 97, 99-101, 103-104, 108-111, 114-115, 117, 119-121, 123-128, 131, 134, 137, 140-142, 144-146, 148-151, 153, 157, 158, 164-165, 167-186, 188-190, and 202-243 have been cited in regard to U.S. Application Serial Number 09/478,916, to which the present application claims priority. In addition, reference numbers 40, 91-92, 98, 106-107, 116, 130, 133, 147, 151-152, 161-163, 187 and 250 have been cited in regard to U.S. Application Serial Number 09/655,010, to which the present application claims priority. Furthermore, reference numbers 46,

70, 96 and 166 have been cited in an International Search Report established in regard to an international application claiming priority to U.S. Application Serial Number 09/655,01.

Applicants submit that these documents, whether taken alone or in combination, fail to show or suggest the claimed subject matter. Applicants request that the Examiner consider the entirety of each document and make them of record in this application. Applicants' submission of these documents for consideration is not to be construed as an admission that the documents qualify as prior art to the claimed subject matter, a representation that a search has been made, nor as an admission that the information is considered to be material to patentability.

Respectfully Submitted,

  
Matthew J. Sampson  
Reg. No. 35,999

Date: October 24, 2003

FORM PTO-1449

(Rev. 12-32)

U.S. Department of Commerce  
Patent and Trademark Office

Atty. Docket No.

Serial No.

00-167-C

09/742,250

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(Use several sheets if necessary)

Applicant:

Werner et al.

Filing Date:

12/20/00

Group:

2819

## U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1.	2,912,684	11/10/59	Steele			
	2.	3,051,901	6/24/58	Yaeger			
	3.	3,078,378	6/28/60	Burley et al.			
	4.	3,267,459	12/18/62	Chomicki et al.			
	5.	3,484,559	7/28/96	Rigby			
	6.	3,508,076	8/26/67	Winder			
	7.	3,510,585	2/2/67	Stone			
	8.	3,560,856	12/26/67	Kaneko			
	9.	3,569,955	3/9/71	Maniere			
	10.	3,571,725	3/23/71	Kaneko			
	11.	3,587,088	6/22/71	Frnszek			
	12.	3,648,064	3/7/72	Mukai et al.			
	13.	3,697,874	10/10/72	Kaneko			
	14.	3,731,199	5/1/73	Tazaki et al.			
	15.	3,733,550	5/15/73	Tazaki et al.			
	16.	3,753,113	8/14/73	Maruta et al.			
	17.	3,754,237	8/21/73	De Laage de Meux			
	18.	3,761,818	9/25/73	Tazaki et al.			

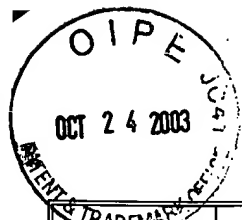
RECEIVED  
NOV -4 2003  
TECHNOLOGY CENTER 2800

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.





## U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	19.	3,772,680	11/13/73	Kawai et al.			
	20.	3,798,544	3/19/74	Norman			
	21.	3,832,490	8/27/74	Leonard			
	22.	3,860,871	1/14/75	Hinoshita et al.			
	23.	3,876,944	4/8/75	Mack et al.			
	24.	3,927,401	12/16/75	McIntosh			
	25.	3,978,284	8/31/76	Yoshino et al.			
	26.	3,988,676	10/26/76	Whang			
	27.	4,038,564	7/26/77	Hakata			
	28.	4,070,650	1/24/78	Ohashi et al.			
	29.	4,086,587	4/25/78	Lender			
	30.	4,097,859	6/27/78	Looschen			
	31.	4,131,761	12/26/78	Giusto			
	32.	4,181,865	1/1/80	Kohyama			
	33.	4,280,221	7/21/81	Chun et al.			
	34.	4,373,152	2/8/83	Jacobsthal			
	35.	4,382,249	5/3/83	Jacobsthal			
	36.	4,403,330	9/6/83	Meyer			
	37.	4,408,135	10/4/83	Yuyama et al.			
	38.	4,408,189	10/4/83	Betts et al.			
	39.	4,438,491	3/20/84	Constant			
	40.	4,481,625	11/6/84	Roberts et al.			
	41.	4,528,550	7/9/85	Graves et al.			
	42.	4,571,735	2/18/86	Furse			
	43.	4,602,374	7/22/86	Nakamura et al.			
	44.	4,620,188	10/28/86	Sengehanh			
	45.	4,628,297	12/9/86	Mita et al			

RECEIVED  
NOV -4 2003  
TECHNOLOGY CENTER 2800

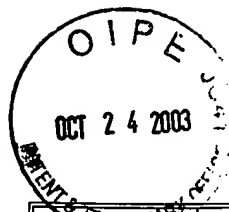
EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

McDONNELL BOEHLEN HULBERT & BERGHOF  
300 SOUTH WACKER DRIVE  
CHICAGO, ILLINOIS 60606  
TELEPHONE (312) 913-0001

MBHB: 00-187-C  
S/N: 09/742,250  
FILING DATE: 12/20/00



## U.S. PATENT DOCUMENTS

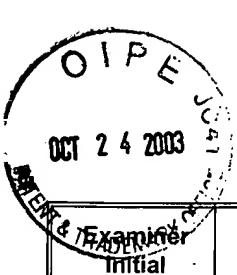
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	46.	4,748,637	5/31/88	Bishop			
	47.	4,779,073	10/18/88	Iketani			
	48.	4,805,190	2/14/89	Jaffre et al.			
	49.	4,821,286	4/11/89	Graczyk et al.			
	50.	4,823,028	4/18/89	Lloyd			
	51.	4,825,450	4/25/89	Herzog			
	52.	4,841,301	6/20/89	Ichihara			
	53.	4,860,309	8/22/89	Costello			
	54.	4,875,049	10/17/89	Yoshida			
	55.	4,888,764	12/19/89	Haug			
	56.	5,003,555	3/26/91	Bergmans			
	57.	5,023,488	6/11/91	Gunning			
	58.	5,023,841	6/11/91	Akrout et al.			
	59.	5,045,728	9/3/91	Crafts			
	60.	5,046,050	9/3/91	Kertis			
	61.	5,115,450	5/19/92	Arcuri			
	62.	5,121,411	6/9/92	Flurharty			
	63.	5,126,974	6/30/92	Sasaki et al.			
	64.	5,153,459	10/6/92	Park et al.			
	65.	5,172,338	12/15/92	Mehrotra et al.			
	66.	5,191,330	3/2/93	Fisher et al.			
	67.	5,194,765	3/16/93	Dunlop et al.			
	68.	5,230,008	7/20/93	Duch et al.			
	69.	5,243,625	9/7/93	Verbakel et al.			
	70.	5,254,883	10/19/93	Horowitz			
	71.	5,259,002	11/2/93	Carlstedt			
	72.	5,280,500	1/18/94	Mazzola et al.			

RECEIVED  
NOV - 4 2003  
TECHNOLOGY  
EXAMINER 2800

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.



## U.S. PATENT DOCUMENTS

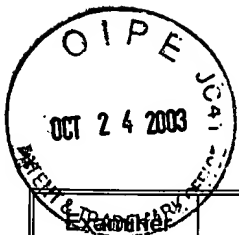
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	73. 5,287,108	2/15/94	Mayes et al			
	74. 5,295,155	3/15/94	Gersbach et al.			
	75. 5,295,157	3/15/94	Suzuki et al.			
	76. 5,315,175	5/24/94	Langner			
	77. 5,331,320	7/19/94	Cideciyan et al			
	78. 5,373,473	12/13/94	Okumura			
	79. 5,408,498	4/18/95	Yoshida			
	80. 5,412,689	5/2/95	Chan et al			
	81. 5,425,056	6/13/95	Maroun et al			
	82. 5,426,739	6/20/95	Lin et al.			
	83. 5,459,749	10/17/95	Park			
	84. 5,471,156	11/28/95	Kim et al.			
	85. 5,473,635	12/5/95	Chevroulet			
	86. 5,483,110	1/9/96	Koide et al.			
	87. 5,438,593	8/1/95	Karam et al.			
	88. 5,508,570	4/16/96	Laber et al.			
	89. 5,513,327	4/30/96	Farmwald et al.			
	90. 5,525,983	6/11/96	Patel et al.			
	91. 5,534,795	7/9/96	Wert			
	92. 5,534,798	7/9/96	Phillips et al.			
	93. 5,539,774	7/23/96	Nobakht et al			
	94. 5,553,097	9/3/96	Dagher			
	95. 5,596,439	1/21/97	Dankberg et al.			
	96. 5,608,755	3/4/97	Rakib			
	97. 5,633,631	5/27/97	Teckman			
	98. 5,663,663	9/2/97	Cao et al.			
	99. 5,640,605	6/17/97	Johnson et al.			

RECEIVED  
NOV - 4 2003  
TECHNOLOGY CENTER

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.



## U.S. PATENT DOCUMENTS

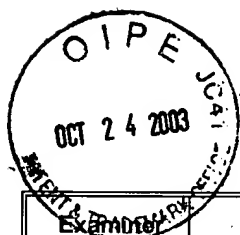
Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	100. 5,644,253	7/1/97	Takatsu			
	101. 5,684,833	11/4/97	Watanabe			
	102. 5,964,424	12/2/97	Ariyavisitakul			
	103. 5,734,294	3/31/98	Bezzam et al.			
	104. 5,740 201	4/14/98	Hui			
	105. 5,742,591	4/21/98	Himayat et al.			
	106. 5,751,168	5/12/98	Speed III et al.			
	107. 5,757,712	5/26/98	Nagel et al.			
	108. 5,761,246	6/2/98	Cao et al.			
	109. 5,793,815	8/11/98	Goodnow et al.			
	110. 5,793,816	8/11/98	Hui			
	111. 5,796,781	8/18/98	DeAndrea et al.			
	112. 5,798,918	8/25/98	Georgiou et al.			
	113. 5,809,033	9/15/98	Turner et al.			
	114. 5,825,825	10/20/98	Altmann et al.			
	115. 5,864,584	1/26/99	Cao et al.			
	116. 5,867,010	2/2/99	Hinedi et al.			
	117. 5,872,468	2/16/99	Dyke			
	118. 5,887,032	3/23/99	Cioffi			
	119. 5,892,466	4/6/99	Walker			
	120. 5,898,734	4/27/99	Nakamura et al.			
	121. 5,917,340	6/29/99	Manohar et al.			
	122. 5,917,856	6/29/99	Torsti			
	123. 5,933,458	8/3/99	Leurent et al.			
	124. 5,942,994	8/24/99	Lewiner et al.			
	125. 5,946,355	8/31/99	Baker			
	126. 5,949,280	9/7/99	Sasaki			

RECEIVED  
NOV 14 2003  
TECHNOLOGY CENTER 2800

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.



## U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Dat	Name	Class	Subclass	Filing Date if Appropriate
	127. 5,969,579	10/19/99	Hartke et al.			
	128. 5,969,648	10/19/99	Garnett			
	129. 5,970,088	10/19/99	Chen			
	130. 5,973,508	10/26/99	Nowak et al.			
	131. 5,977,798	11/2/99	Zerbe			
	132. 5,982,741	11/9/99	Ethier			
	133. 5,986,472	11/16/99	Hinedi et al.			
	134. 6,005,895	12/21/99	Perino et al.			
	135. 6,006,169	12/21/99	Sandhu et al.			
	136. 6,009,120	12/28/99	Nobakht			
	137. 6,018,550	1/25/00	Emma et al			
	138. 6,034,993	3/7/00	Norrell et al.			
	139. 6,038,260	3/14/00	Emma et al			
	140. 6,048,931	4/11/00	Fujita et al.			
	141. 6,049,229	4/11/00	Manohar et al			
	142. 6,052,390	4/18/00	Deliot et al			
	143. 6,061,395	5/9/00	Tonami			
	144. 6,067,326	5/23/00	Jonsson et al.			
	145. 6,078,627	6/20/00	Crayford			
	146. 6,094,461	7/25/00	Heron			
	147. 6,097,215	8/1/00	Bialas Jr et al			
	148. 6,101,561	8/8/00	Beers et al.			
	149. 6,114,979	9/5/00	Kim			
	150. 6,122,010	9/19/00	Emelko			
	151. 6,140,841	10/31/00	Suh			
	152. 6,160,421	12/12/00	Barna			
	153. 6,195,397	2/27/01	Kwon			

RECEIVED  
NOV - 14 2003  
TECHNOLOGY CENTER-2800

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.



# U.S. PATENT DOCUMENTS

Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	154. 6,204,785	3/20/01	Fattaruso			
	155. 6,215,635	4/10/01	Nguyen			
	156. 6,222,380	4/24/01	Gerowitz			
	157. 6,307,824	10/23/01	Kuroda et al			
	158. RE 30,182	12/25/79	Howson			
	159. 5,825,450	10/28/98	Date et al.			
	160. 5,604,468	2/18/97	Gillig			
	161. 5,546,042	8/13/96	Tedrow et al.			
	162. 6,094,075	7/25/00	Garrett Jr et al.			
	163. 6,069,577	5/30/00	Morisson et al.			

## FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
164.	WO 95/31867	11/23/95	PCT				
165.	WO 96/31038	10/3/96	PCT				
166.	WO 99/10982	3/4/99	PCT				
167.	EP 0 352 869	1/31/90	EP				
168.	EP 0 482 392 with translation	4/29/92	EP				
169.	EP 0 490 504	7/17/92	EP				
170.	EP 0 094 624	11/23/83	EP				
171.	43 20 930	1/5/95	DE				
172.	358070662	4/27/83	JP				
173.	362051329	3/6/87	JP				
174.	354051343	4/23/79	JP				
175.	356164650	12/17/81	JP				
176.	359036465	2/28/84	JP				

RECEIVED  
 NOV - 4 2003  
 TECHNOLOGY CENTER 2800

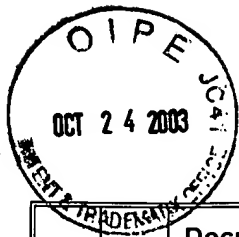
EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

McDONNELL BOEHNNEN HULBERT & BERGHOF  
 300 SOUTH WACKER DRIVE  
 CHICAGO, ILLINOIS 60606  
 TELEPHONE (312) 913-0001

MBHB: 00-167-C  
 S/N: 09/742,250  
 FILING DATE: 12/20/00



## FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
177.	360087551	5/17/85	JP				
178.	360194647	10/3/85	JP				
179.	408286943	11/1/96	JP				
180.	409181778	7/11/97	JP				
181.	354060850	5/16/79	JP				
182.	408202677	8/9/96	JP				
183.	405143211	6/11/93	JP				
184.	404044691	2/14/92	JP				
185.	402140676	5/30/90	JP				
186.	402128201	5/16/90	JP				
187.	10200345	7/13/98	JP				
188.	WO 98/33306	7/30/98	PCT				
189.	EP 0 463 316	1/2/92	EP				
190.	58-54412	3/3/83	JP				

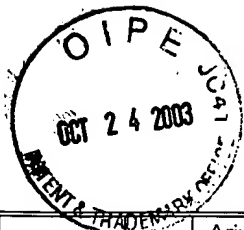
## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

191.	IEEE Standard 802.3ad-1999, 802.3 Supplemental. Local and Metropolitan Area Networks, July 17, 1999
192.	802.3 ab., A Tutorial Presentation, 63 pages, presented at an IEEE 802.3 working group meeting in March 1998.
193.	Thompson, "How 1000BASE-T Works", <i>IEEE 802.3 Plenary</i> , (1997), Montreal PQ Canada, 8 pages
194.	Perez-Alvarez, et al. "A Differential Error Reference Adaptive Echo Canceller for Multilevel PAM Line Codes", <i>IEEE</i> , pp. 1707-1710 (1996).
195.	Kuczyski, et al., "A 1Mb/s Digital Subscriber Line Transceiver Signal Processor", <i>1993 IEEE International Solid-State Circuits Conference</i> , (1993)
196.	Cova, et al. "Characterization of Individual Weights in Transversal Filters and Application to CCD's", <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-17, pp. 1054-1061 (1982).
197.	Dally, et al., "Multi-Gigabit Signaling with CMOS", May 12, 1997.
198.	Fielder, et al. "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," <i>1997 IEEE International Solid State Circuit Conference and Slideset</i> .
199.	Raghavan, et al. "Nonuniformly Spaced Trapped Delay-Line Equalizers", <i>IEEE Transactions on Communications</i> , Vol. 41, pp. 1290-1295 (1993).
200.	Ariyavisitakul, et al., "Reduced-Complexity Equalization Techniques for Broadband Wireless Channels", <i>IEEE Journal on Selected Areas in Communication</i> , pp. 5-15 (1997)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.



## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

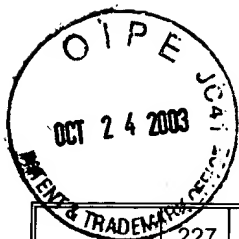
201.	Ariyavisitakul, et al., "Tap-Selected Decision-Feedback Equalization", <i>IEEE Transactions on Communications</i> , pp. 1497-1500 (1997).
202.	Sidiropoulos, et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 32, pp. 681-690 (1997).
203.	Donnelly et al, "A 660 MB/s Interface Megacell Portable Circuit in 0.3 $\mu$ m-0.7 $\mu$ m CMOS ASIC", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 31, pp. 1995-2003 (1996).
204.	Allen, "Probability, Statistics, and Queueing Theory with Computer Science Applications," 2 <sup>nd</sup> Edition, CH 7, pp.450-459.
205.	Chappell, et al., "A 2ns-Cycle, 4ns Access 512kb CMOS ECL SRAM", 1991 <i>IEEE Journal of Solid-State Circuits</i> , pp. 50-51 (1991).
206.	Pilo, et al., "A 300MHz, 3.3V 1Mb SRAM Fabricated in a .5 $\mu$ m CMOS Process," <i>IEEE Journal of Solid-State Circuits</i> , pp. 148-149 (1996).
207.	Schumacher, et al., "CMOS Subnanosecond True-ECL Output Buffer", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 25, pp. 150-154 (1990).
208.	Yang, et al., "A 4-ns 4Kx1-bit Two Port BiCMOS SRAM", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 23, No. 5, pp. 1030-1040 (1988).
209.	Bazes, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", <i>IEEE Journal of Solid State Circuits</i> , Vol. 28, pp. 165-168, (1991).
210.	Ishibe, et al. "High-Speed CMOS I/O Buffer Circuits", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 27, pp. 671-677 (1992).
211.	Lee, et al., "A 80ns 5V-Only Dynamic RAM", <i>ISSCC/79 Proceedings</i> , Paper 12.2 (1979).
212.	Seki, et al., "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 28, pp. 483 (1993).
213.	Kobayashi, et al., "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture", <i>IEEE Journal of Solid State Circuits</i> , pp. 523-527 (1993).
214.	Tomassini et al., "A fully differential CMOS Line Driver for ISDN", <i>IEEE Journal of Solid State Circuits</i> , Vol. 25, No. 2 (1990).
215.	Farjad-Rad, et al., "A 0.4 $\mu$ m CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 34, pp. 580-585 (1999).
216.	Yeung, et al., "A 2.4Gbps Per Pin Simultaneous Bidirectional Parallel Link with Per Pin Skew Compensation", <i>ISSCC 2000</i> , pp. 1-11
217.	Portmann et al., "A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRaMs", <i>IEEE VLSI Circuits Symposium</i> , June 1999.
218.	Moncayo, "Bus Design and Analysis at 500 MHz and Beyond", <i>High Performance System Design Conference</i> , (1995).
219.	Lau, et al. "A 2.6-Byte/s Multipurpose Chip-to-Chip Interface", <i>IEEE Journal of Solid State Circuits</i> , Vol. 33, pp. 1617-1626 (1998).
220.	Current, "Current Mode CMOS Multiple-Valued Logic Circuits", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 29, No. 2, pp. 95-107 (1994).
221.	Dally and Poulton, <i>Digital Systems Engineering</i> , Cambridge University Press, New York, pp. 334-347 and 352 (1998).
222.	Farjad-Rad, et al. "An Equalization Scheme for 10Gb/s 4-PAM Signaling over Long Cables," <i>Department of Electrical Engineering, Stanford University</i> , 1997
223.	IBM Technical Disclosure Bulletin, June 1967, "Use of Multibit encoding to increase Linear Recording Densities in Serially Recorded Records," pp. 14-15.
224.	IBM Technical Disclosure Bulletin, Jan. 1968, "Coding Data Transmission," pp. 1295-1296.
225.	IBM Technical Disclosure Bulletin, July 1969, "Clock Recovery Circuit," pp. 219-220.
226.	IBM Technical Disclosure Bulletin, November 1970, "Transmission by Data Encoding", pp. 1519-1520.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.





## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

227.	IBM Technical Disclosure Bulletin, Feb. 1976, "Bidirectional Communications Within a Binary Switching System," pp. 2865-2866
228.	IBM Technical Disclosure Bulletin, Feb. 1976, "Multilevel Bidirectional Signal Transmission," pp. 2867-2868
229.	IBM Technical Disclosure Bulletin, October 1978, "Multilevel Signal Transfers," pp. 1798-1800
230.	IBM Technical Disclosure Bulletin, Feb. 1981, "Circuit for Multilevel Logic Implementation," pp. 4206-4209
231.	IBM Technical Disclosure Bulletin, April 1983, "Multi Level Logic Testing", pp. 5903-5904.
232.	IBM Technical Disclosure Bulletin, September 1985, "Push-Pull Multi-Level Driver Circuit for Input-Output Bus," pp. 1649-1651
233.	IBM Technical Disclosure Bulletin, Aug. 1986, "Multilevel CMOS Sense Amplifier," pp. 1280-1281.
234.	IBM Technical Disclosure Bulletin, Nov. 1992, "Multi-Level Encoded High Bandwidth Bus," pp. 444-447.
235.	IBM Technical Disclosure Bulletin, Feb. 1995, "High Speed Complimentary Metal Oxide Semiconductors Input/Output Circuits," pp. 111-114.
236.	IBM Technical Disclosure Bulletin, April 1995, "Common Front End Bus for High-Performance Chip-to-Chip Communication," pp. 443-444
237.	IBM Technical Disclosure Bulletin, April 1995, "High Performance Impedance Controlled CMOS Driver," pp. 445-448.
238.	IBM Technical Disclosure Bulletin, April 1995, "3-state Decoder for External 3-State Buffer," pp. 477-478.
239.	Matick, Transmission Lines for Digital and Communication Networks: An Introduction to Transmission Lines, High-Frequency and High-Speed Pulse Characteristics and Applications, IEEE Press, New York, pp. 268-269 (1995).
240.	Singh, "Four Valued Buses for Clocked CMOS VLSI Systems", <i>Proceedings of the Seventeenth International Symposium on Multiple-Valued Logic, The Computer Society of the IEEE</i> , pp. 128-133 (1987).
241.	Smith, "The Prospects for Multivalued Logic: a Technology and Applications View", <i>IEEE Transactions on Computers</i> , Vol. c-30, pp. 619-634 (1981).
242.	Thrion, "10 Gig PMD Technologies," <i>IEEE Plenary</i> , Kauai, Hawaii, (1999).
243.	Vranesic, "Multivalued Signalling in Daisy Chain Bus Control", <i>Proceedings of the Ninth International Symposium on Multiple-Valued Logic</i> , Bath, England, pp. 14-18 (1979).
244.	Azadet et al., "A Gigabit Transceiver Chip Set for UTP CAT6 Cables in Digital CMOS Technology," <i>2000 IEEE International Solid State Circuits Conference</i> , pp. 3-6-307.
245.	Yang, et al., "A Scalable 32Gb/s Parallel Data Transceiver with On-Chip Timing Calibration Circuits", <i>2000 IEEE International Solid-State Circuits Conference</i> , pp. 258-259 (2000).
246.	Modulation Schemes for High Bit Rate Data Transmission in the Loop Plant, URL- <a href="http://www.bib.fri-lippe.de/volltext/dipl/schlegd/chapter4.html">http://www.bib.fri-lippe.de/volltext/dipl/schlegd/chapter4.html</a> , 29 pages, printed 4/19/01
247.	Scott, "Propagation Over Multiple Parallel Transmission Lines Via Modes", IBM Technical Disclosure Bulletin, April 1990.
248.	1996 Symposium on VLSI Circuits, <i>IEEE</i> , June 13-15, 1996
249.	Taborek, et al. IEEE 802.3 Tutorial, "Multi-Level Analog Signaling Techniques for 10 Gigabit Ethernet",.
250.	IMB, Servo Control of Analog Power Supplies Interface Card, 4/1/1993, Vol. 36, Issue 4, pp. 283-286.

RECEIVED  
NOV - 4 2003  
TECHNOLOGY CENTER 2800

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.